IN THE SPECIFICATION:

Please replace paragraph number **[0001]** with the following rewritten paragraph:

[0001] ~~Cross-Reference~~ Cross-Reference to Related Applications: This application is a continuation of application Serial No. 09/392,153, filed September 8, 1999, now U.S. Patent ~~6,265,775 B1~~ 6,265,775, issued July 24, 2001, which is a divisional of application Serial No. 08/788,209, filed January 24, 1997, now U.S. Patent ~~6,221,753 B1~~ 6,221,753, issued April 24, 2001.

Please replace paragraph number **[0005]** with the following rewritten paragraph:

[0005] There are numerous variations to the standard flip chip attachment technique. For example, U.S. Patent 5,329,423 issued July 12, 1994 to Scholz relates to a demountable ~~flip chip~~ flip-chip assembly comprising a first substrate having a contact site with a raised bump and a second substrate having a depression for a contact site. The raised bumps are pressed into the depressed areas to electrically and mechanically connect the first substrate to the second substrate without using reflowed solder. Thus, the first substrate can be removed from the second substrate without damaging either substrate.

Please replace paragraph number **[0009]** with the following rewritten paragraph:

[0009] As an electronic package dissipates heat to its surroundings during operation, or as the ambient system temperature changes, differential thermal expansions cause stresses to be generated in the interconnection structure (solder ball bonds) between the semiconductor die and the substrate. These stresses produce instantaneous elastic and, most often, plastic strain, as well as time-dependent (plastic and ~~anelastic~~ elastic) strains in the interconnection structure, particularly at the weakest interconnection structure. Thus, the thermal expansion mismatch between chip and substrate will cause a shear displacement to be applied on each terminal which can fracture the solder connection.

Please replace paragraph number **[0017]** with the following rewritten paragraph:

[0017] A passivation layer is applied over the second substrate active surface. The passivation layer is preferably thicker than the height of the second substrate conductive bumps. The passivation layer is etched by any known industry standard technique to form vias to expose an active surface of the second substrate conductive bump. It is, of course, understood that, rather than etching the passivation layer, a masking technique could be employed, such as a silk screen, over the semiconductor die conductive pad facing surface when applying the passivation layer.

Please replace paragraph number **[0033]** with the following rewritten paragraph:

[0033] FIG. 4 illustrates a first alternative first substrate/second substrate assembly 400 of the present invention. The first ~~alternate~~ alternative first substrate/second substrate assembly 400 is similar to the first substrate/second substrate assembly 300 of FIG. 3; therefore, components common to FIG. 3 and FIG. 4 retain the same numeric designation. The first alternative first substrate/second substrate assembly 400 differs from the first substrate/second substrate assembly 300 in that the second substrate or flip-chip component 200 is specifically a substrate with the conductive pad 214 formed on a substrate lead 408, rather than on a ~~flip-chip~~ flip-chip type bond pad 204 connected to a trace lead 208 shown in FIG. 3. The first alternative first substrate/second substrate assembly 400 also differs from the first substrate/second substrate assembly 300 in that the passivation layer 216 is first applied to first substrate facing surface 106, then a layer of adhesive 402 is disposed between the passivation layer 216 and the second substrate 202.

Please replace paragraph number **[0034]** with the following rewritten paragraph:

[0034] FIG. 5 illustrates a second alternative first substrate/second substrate assembly 500 of the present invention. The second ~~alternate~~ alternative first substrate/second substrate assembly 500 is similar to the first substrate/second substrate assembly 300 of FIG. 3; therefore, components common to FIG. 3 and FIG. 5 retain the same numeric designation. The second alternative first substrate/second substrate assembly 500 differs from the first

substrate/second substrate assembly 300 in that a glob top material 502 is used to attach the second substrate or flip-chip component 200 to the first substrate component 100, rather than using the layer of adhesive 302 shown in FIG. 3.

Please replace paragraph number **[0035]** with the following rewritten paragraph:

[0035] FIG. 6 illustrates a third alternative first substrate/second substrate assembly 600 of the present invention. The third ~~alternate~~ alternative first substrate/second substrate assembly 600 is similar to the first substrate/second substrate assembly 300 of FIG. 3; therefore, components common to FIG. 3 and FIG. 6 retain the same numeric designation. The third alternative first substrate/second substrate assembly 600 differs from the first substrate/second substrate assembly 300 in that an encapsulant material 602 is used to substantially encase and attach the second substrate or flip-chip component 200 together with the first substrate component 100, rather than using the layer of adhesive 302 shown in FIG. 3.

Please replace paragraph number **[0036]** with the following rewritten paragraph:

[0036] FIG. 7 illustrates a fourth alternative first substrate/second substrate assembly 700 of the present invention. The fourth ~~alternate~~ alternative first substrate/second substrate assembly 700 is similar to the first substrate/second substrate assembly 300 of FIG. 3; therefore, components common to FIG. 3 and FIG. 7 retain the same numeric designation. The fourth alternative first substrate/second substrate assembly 700 differs from the first substrate/second substrate assembly 300 in that a first plurality of grooves 702 is disposed on the facing surface 106 of the first substrate 102 and a second plurality of grooves 704 is disposed on the facing surface 206 of the second substrate 202 wherein the first plurality of grooves 702 intermesh with the second plurality of grooves 704 to assist in preventing or minimizing the movement of first substrate 102 and/or second substrate 202 due to thermal expansion or other mechanical causes.